Listing of claims:

1. (Currently Amended) A clock free apparatus for sampling an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

a timing delay circuit ~~is~~ arranged to produce at least two strobe signals in response to the input signal such that the at least two strobe signals each have a corresponding pulse width ~~pulse-widths~~ that are no greater than ~~within~~ the pulse-width ~~of~~ associated with the input signal;

a comparator circuit ~~is~~ arranged to produce a comparator output signal in response to a comparison between the input signal and a reference level signal; and

a sampling logic ~~is~~ arranged to sample at least two data points within a sampling window in response to the at least two strobe signals and the comparator output signal, the sampling window having edges that correspond to the pulse-width of the input signal such that the at least two sampled data points correspond to at least two samples from the comparator output signal over the time period associated with the pulse-width of the input signal.

2. (Original) A clock free apparatus as in Claim 1, wherein the input signal is a differential input signal, the reference level signal is a differential peak level signal, and the comparator circuit is arranged to produce the comparator output signal in response to a comparison between the differential input signal and the differential peak level signal.

3. (Original) A clock free apparatus as in Claim 1, wherein the input signal is a differential input signal that includes a top input signal and a bottom input signal, the reference level signal is a differential peak level signal that includes a top peak level signal and a bottom peak level signal, and the comparator circuit is arranged such that the comparator output signal is a first logic level when the top input signal exceeds the top peak level signal, the comparator output signal is the first logic level when the bottom input signal drops below the bottom peak level signal, and the comparator output signal is a second logic level that is different from the first logic level when the top equalized signal is below the top peak level signal and the bottom equalized signal is above the bottom peak level signal.

4. (Original) A clock free apparatus as in Claim 1, further comprising a top peak generator circuit and a bottom peak generator circuit, wherein the input signal is a differential input signal including a top input signal and a bottom input signal, the reference level signal is a differential peak level signal including a top peak level signal and a bottom peak level signal, and the top peak level signal is produced by the top peak generator circuit and the bottom peak level signal is produced by the bottom peak generator circuit.

5. (Currently Amended) A clock free apparatus ~~as in Claim 1~~ for sampling an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

a timing delay circuit is arranged to produce strobe signals in response to the input signal such that the strobe signals have pulse-widths that are within the pulse width of the input signal;

a comparator circuit is arranged to produce a comparator output signal in response to a comparison between the input signal and a reference level signal; and

a sampling logic is arranged to sample data points within a sampling window in response to the strobe signals and the comparator output signal, the sampling window having edges that correspond to the pulse-width of the input signal such that the sampled data points correspond to samples from the comparator output signal, wherein the strobe signals generated by the timing delay circuit include a first strobe signal and a second strobe signal, the first strobe signal is a first logic pulse that is responsive to rising and falling edges of the input signal, and the second strobe signal is another logic pulse that occurs a predetermined time delay after one of the rising and falling edges of the input signal such that the logic pulse and the another logic pulse occur within the pulse-width of the input signal.

6. (Original) A clock free apparatus as in Claim 5, wherein the comparator circuit includes a reset control input that is coupled to the first strobe signal such that the output of the comparator is periodically reset to a first logic level, and the output of the comparator indicates a second logic level that is different from the first logic level when the input signal exceeds the reference level signal.

7. (Currently Amended) A clock free apparatus as in Claim 5, the sampling logic further comprising:

a first logic circuit ~~is~~ arranged to produce a first output signal that is periodically reset to a first logic level in response to the second strobe signal, wherein the first output signal toggles between the first logic level and the second logic level in response to the comparator output signal;

a second logic circuit ~~is~~ arranged to produce a second output signal that follows the first output signal in response to the first strobe signal;

a third logic circuit ~~is~~ arranged to produce a third output signal that follows the second output signal in response to the second strobe signal, wherein the third output signal corresponds to a first of the sampled data points; and

a fourth logic circuit ~~is~~ arranged to produce a fourth output signal that follows the output of the comparator in response to the second strobe signal, wherein the fourth output signal corresponds to a second of the sampled data points.

8. (Currently Amended) A clock free apparatus as in Claim 1, wherein the at least two sampled data points indicate a condition of the input signal that corresponds to at least one of an under-shoot condition, an over-shoot condition, an under-amplitude condition, and an over-amplitude condition.

9. (Currently Amended) A clock free apparatus ~~as in Claim 1~~ for sampling an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

a timing delay circuit is arranged to produce strobe signals in response to the input signal such that the strobe signals have pulse-widths that are within the pulse width of the input signal;

a comparator circuit is arranged to produce a comparator output signal in response to a comparison between the input signal and a reference level signal; and

a sampling logic is arranged to sample data points within a sampling window in response to the strobe signals and the comparator output signal, the sampling window having edges that

correspond to the pulse-width of the input signal such that the sampled data points correspond to samples from the comparator output signal, wherein the sampled data points include a first sampled data point and a second sampled data point, the first sampled data point corresponding to a sample of the comparator output signal after the first edge of the input signal, and the second sampled data point corresponding to another sample of the comparator output signal in response to at least one of the strobe signals such that the sampled data points correspond to samples of the input signal that are within the pulse-width of the input signal.

10. (Original) A clock free apparatus as in Claim 9, wherein the condition of the input signal is an over-amplitude condition when the first sampled data point indicates a first logic level and the second sampled data point indicates the first logic level, and condition of the input signal is an under-amplitude condition when the first sampled data point indicates a second logic level that is different from the first logic level and the second sampled data point indicates a second logic level.

11. (Original) A clock free apparatus as in Claim 9, wherein the condition of the input signal is an over-shoot condition when the first sampled data point indicates a first logic level and the second sampled data point indicates a second logic level that is different from the first logic level, and the condition of the input signal is an under-shoot condition when the first sampled data point indicates a second logic level and the second sampled data point indicates the first logic level for the persistent time interval.

12. (Original) A clock free apparatus as in Claim 1, further comprising:

an equalizer circuit that produces an equalized signal in response to a received signal; and

a data slicer circuit that produces the input signal in response to the equalized signal, the input signal corresponding to a digital representation of the equalized signal.

13. (Currently Amended) A clock free method for sampling an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

comparing the input signal to a peak level signal to produce a comparator output signal;

generating a first and second timing signal from the input signal, wherein the first and second timing signals are within the pulse-width of the input signal;

sampling a first data point from the comparator output in response to the ~~comparator output~~ first timing signal;

sampling a second data point from the comparator output in response to ~~a~~ the second timing signal, wherein the first and second data points correspond to sample points that are within the pulse-width of the input signal.

14. (Original) A clock free method as in Claim 13, sampling the first data point further comprising:

triggering a first memory circuit in response to the comparator output signal;

resetting the first memory circuit in response to the second timing signal;

coupling an output of the first memory circuit to an input of a second memory circuit;

triggering the second memory circuit in response to the first timing signal;

coupling an output of the second memory circuit to an input of a third memory circuit; and

triggering the third memory circuit in response to the second timing signal such that an output of the third memory circuit corresponds to the first data point.

15. (Original) A clock free method as in Claim 13, sampling the second data point further comprising triggering a memory circuit in response to the second timing signal such that an output of the memory circuit follows the comparator output signal when triggered, the output of the memory circuit corresponding to the second data point.

16. (Original) A clock free method as in Claim 14, further comprising resetting the first, second, and third memory circuit in response to a reset control signal.

17. (Original) A clock free system for sampling an input signal that has a pulse-width defined between a first edge and a second edge, comprising:

a means for producing data produces a data signal in response to the input signal, the data signal corresponding to a digital representation of the input signal;

a means for producing a first timing signal produces a first timing signal in response to the data signal, wherein the first timing signal is a pulse that occurs a first time delay after a change in the data signal between a logic state and an other logic state;

a means for producing a second timing signal produces a second timing signal in response to the data signal, wherein the second timing signal is a pulse that occurs a second time delay after the data signal changes from the logic state to the other logic state, and the pulses of the first timing signal and the second timing signal are within the pulse-width of the input signal;

a means for comparing produces a comparator output signal in response to a comparison between the input signal and a reference level signal; and

a means for sampling data points produces a first sampled data point in response the comparator output signal and the first and second strobe signals, the means for sampling also produces a second sampled data point in response to the comparator output signal and at least one of the first and second strobe signals, wherein the first and second sampled data points correspond to sampled data points within the pulse-width of the input signal.

18. (Original) A clock free system as in Claim 17, the means for sampling data points further comprising a means for triggering a fourth memory circuit in response to the second timing signal such that an output of the fourth memory circuit follows the comparator output signal when triggered, the output of the fourth memory circuit corresponding to the second data point.

19. (Original) A clock free system as in Claim 18, the means for sampling data points further comprising:

a means for triggering a first memory circuit in response to the comparator output signal;

a means for resetting the first memory circuit in response to the second timing signal;

a means for coupling an output of the first memory circuit to an input of a second memory circuit;

a means for triggering the second memory circuit in response to the first timing signal;

a means for coupling an output of the second memory circuit to an input of a third memory circuit; and

a means for triggering the third memory circuit in response to the second timing signal such that an output of the third memory circuit corresponds to the first data point.

20. (Original) A clock free system as in Claim 19, further comprising a means for resetting the means for comparing in response to the first timing signal.